

FIG. 1
(Prior Art)

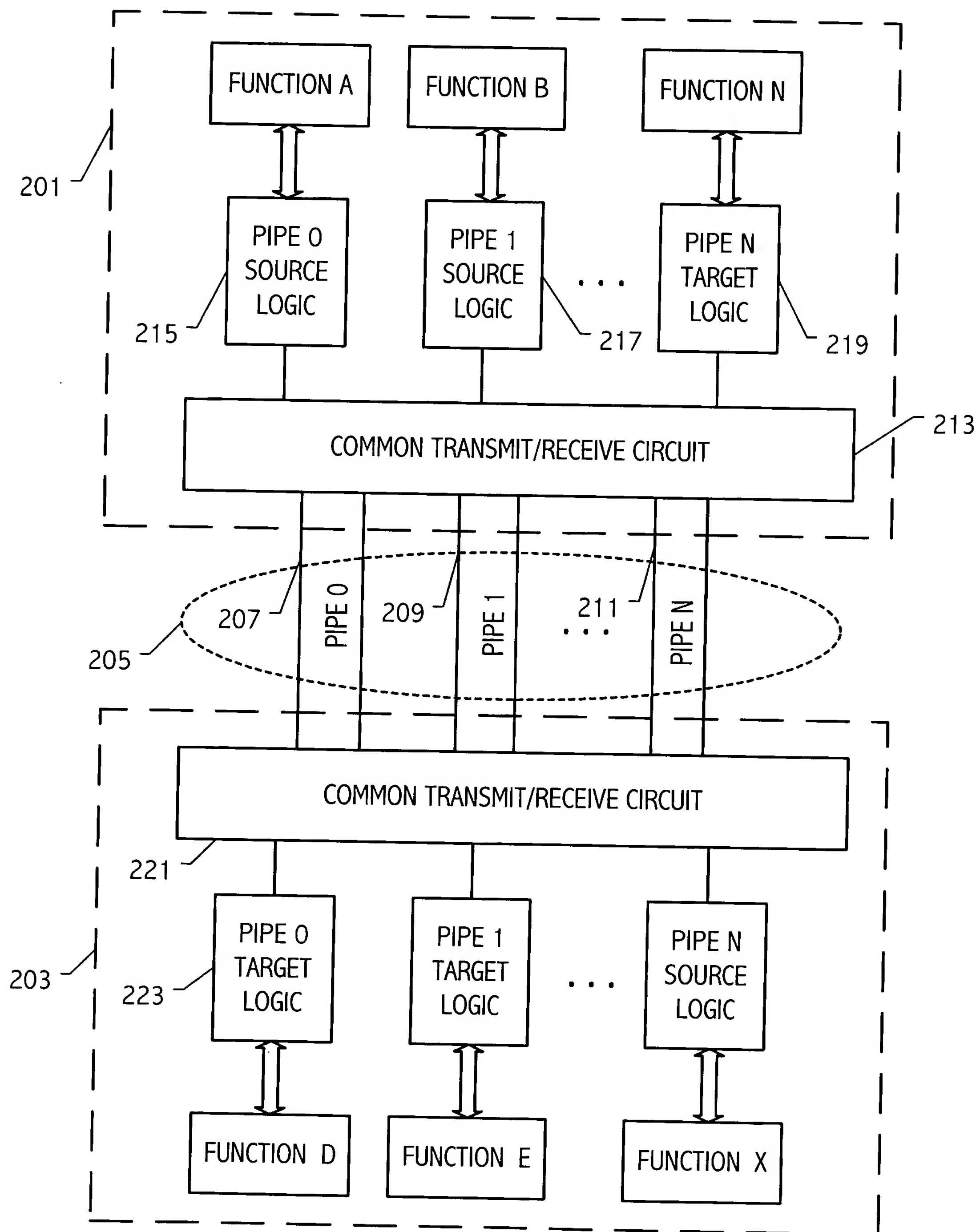


FIG. 2

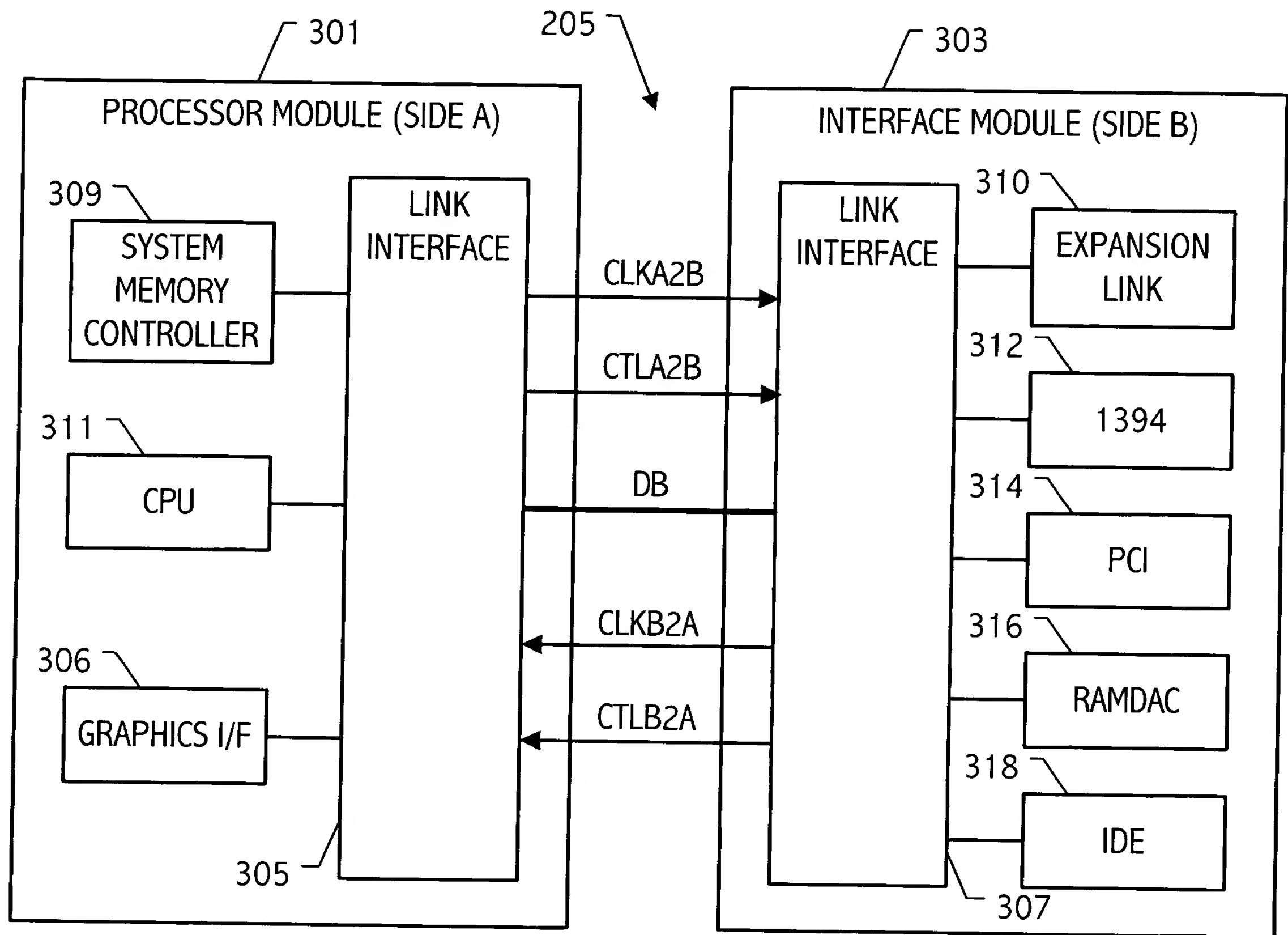


FIG. 3

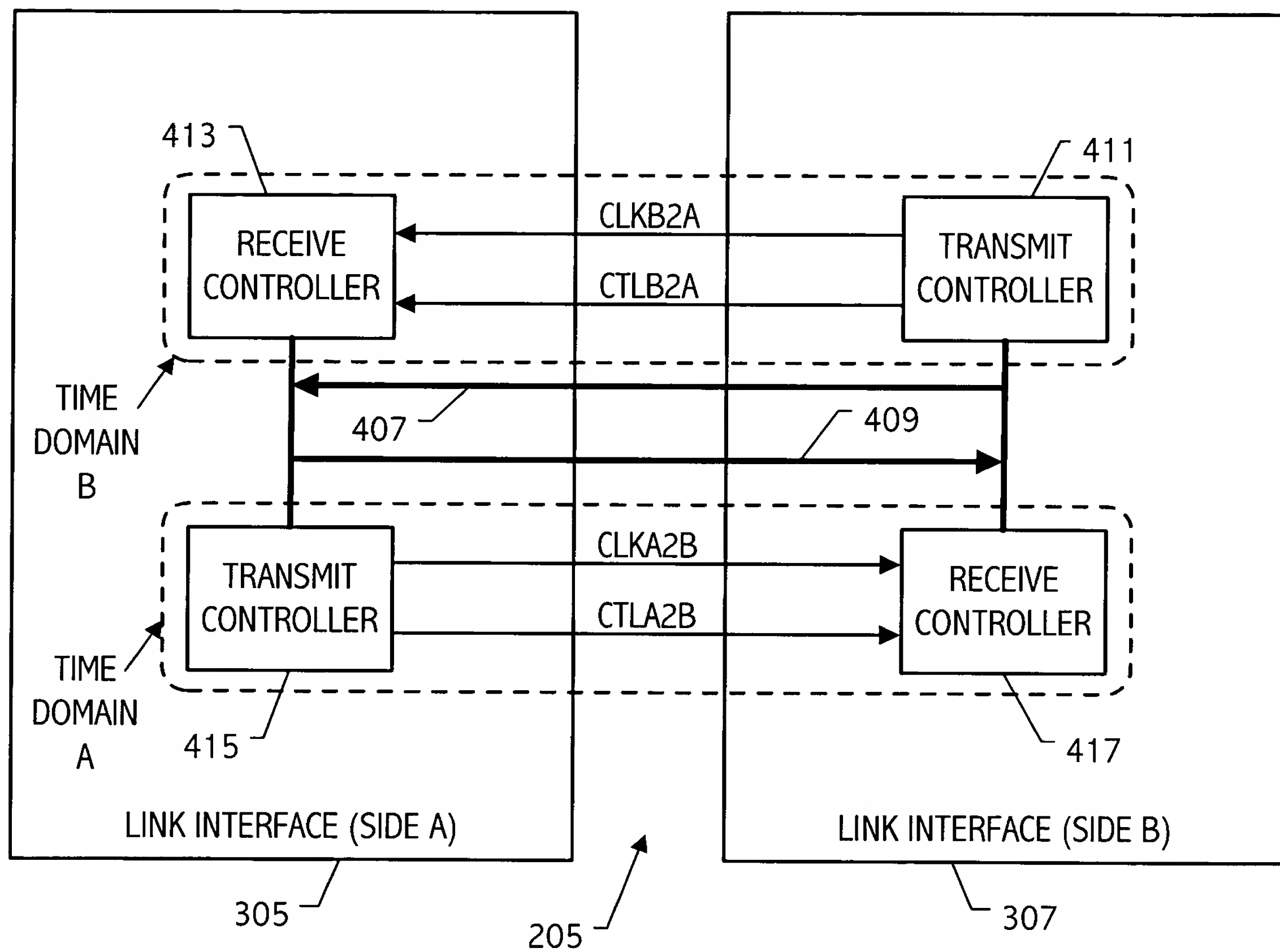


FIG. 4

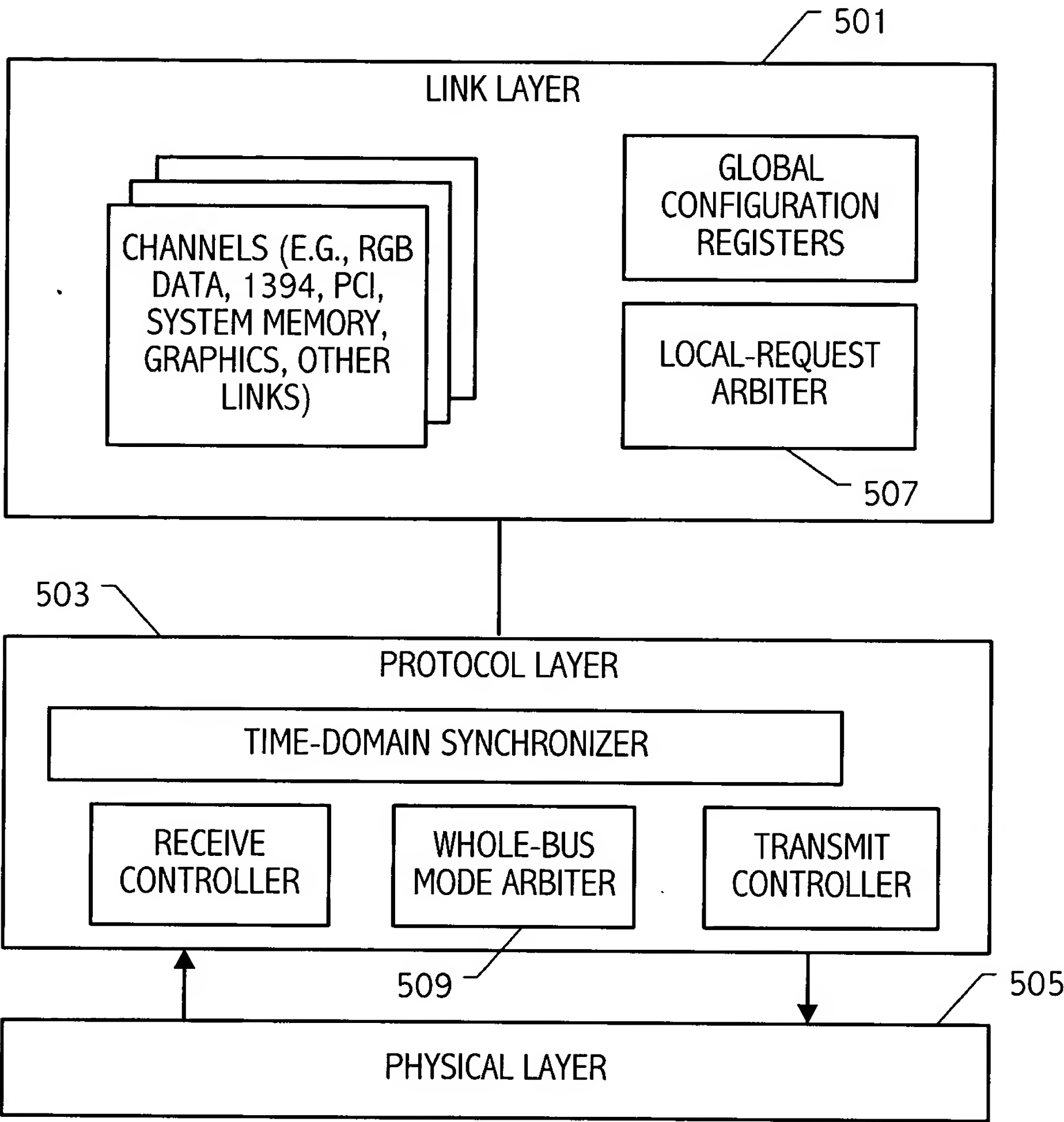


FIG. 5

START	END	NAME	DESCRIPTION
FE 0200 0000	FE FFFF FFFF	RESERVED	
FE 0100 0000	FE 01FF FFFF	CONFIGURATION	24-BIT CONFIGURATION SPACE
FE 0001 0000	FE 00FF FFFF	RESERVED	
FE 0000 0000	FE 0000 FFFF	x86 I/O	16-BIT x86 I/O ADDRESS SPACE
00 0000 0000	FD FFFF F FFF	NORMAL MEMORY	DRAM ADDRESS SPACE
00 0000 0000	00 FFFF FFFF	PCI MEMORY	32-BIT PCI ADDRESS SPACE

FIG. 6

MEMORY WRITE PACKET

PIPE ID # (5)	PKT TYPE (6)	TAG (5)	BUF AVAIL (4)	RSRVD (4)	ADDR (40)	RSRVD (2)	SIZE (6)	DATA (1-64)
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FIG.
7A

SPECIAL CYCLE WRITE PACKET

PIPE ID # (5)	PKT TYPE (6)	TAG (5)	BUF AVAIL (4)	RSRVD (4)	ADDR (40)	RSRVD (2)	SIZE (6)	DATA (4)
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FIG.
7B

NON- ADDRESSED WRITE PACKET

PIPE ID # (5)	PKT TYPE (6)	TAG (5)	BUF AVAIL (4)	RSRVD (4)	RSRVD (2)	SIZE (6)	DATA (1-64)
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FIG.
7C

WRITE ACK (OR NAK) PACKET

PIPE ID # (5)	PKT TYPE (6)	TAG (5)	BUF AVAIL (4)	RSRVD (4)
---------------	--------------	---------	---------------	-----------

FIG.
7D

FLUSH PACKET

PIPE ID # (5)	PKT TYPE (6)	RSRVD (5)	BUF AVAIL (4)	RSRVD (4)
---------------	--------------	-----------	---------------	-----------

FIG.
7E

FENCE PACKET

PIPE ID # (5)	PKT TYPE (6)	RSRVD (5)	BUF AVAIL (4)	RSRVD (4)
---------------	--------------	-----------	---------------	-----------

FIG.
7F

MEMORY READ REQUEST PACKET

PIPE ID # (5)	PKT TYPE (6)	TAG (5)	BUF AVAIL (4)	RSRVD (4)	ADDR (40)	RSRVD (2)	SIZE (6)
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FIG.
7G

NON-ADDRESSED READ REQUE ST PACKET

PIPE ID # (5)	PKT TYPE (6)	RSRVD (1)	BUF AVAIL (4)	RSRVD (2)	SIZE (6)
---------------	--------------	-----------	---------------	-----------	----------

FIG.
7H

READ RESPONSE PACKET

PIPE ID # (5)	PKT TYPE (6)	TAG (5)	BUF AVAIL (4)	RSRVD (4)	RSRVD (2)	SIZE (6)	DATA (1-64)
---------------	--------------	---------	---------------	-----------	-----------	----------	-------------

FIG.
7I

NON-ADDRESSED READ R ESPONSE PACKET

PIPE ID # (5)	PKT TYPE (6)	RSRVD (1)	BUF AVAIL (4)	RSRVD (2)	SIZE (6)	DATA (1-64)
---------------	--------------	-----------	---------------	-----------	----------	-------------

FIG.
7J

READ REJECT PACKET

PIPE ID # (5)	PKT TYPE (6)	TAG (5)	BUF AVAIL (4)	RSRVD (4)
---------------	--------------	---------	---------------	-----------

FIG.
7K

NOP PACKET

PIPE ID # (5)	PKT TYPE (6)	RSRVD (5)	BUF AVAIL (4)	RSRVD (4)
---------------	--------------	-----------	---------------	-----------

FIG.
7L

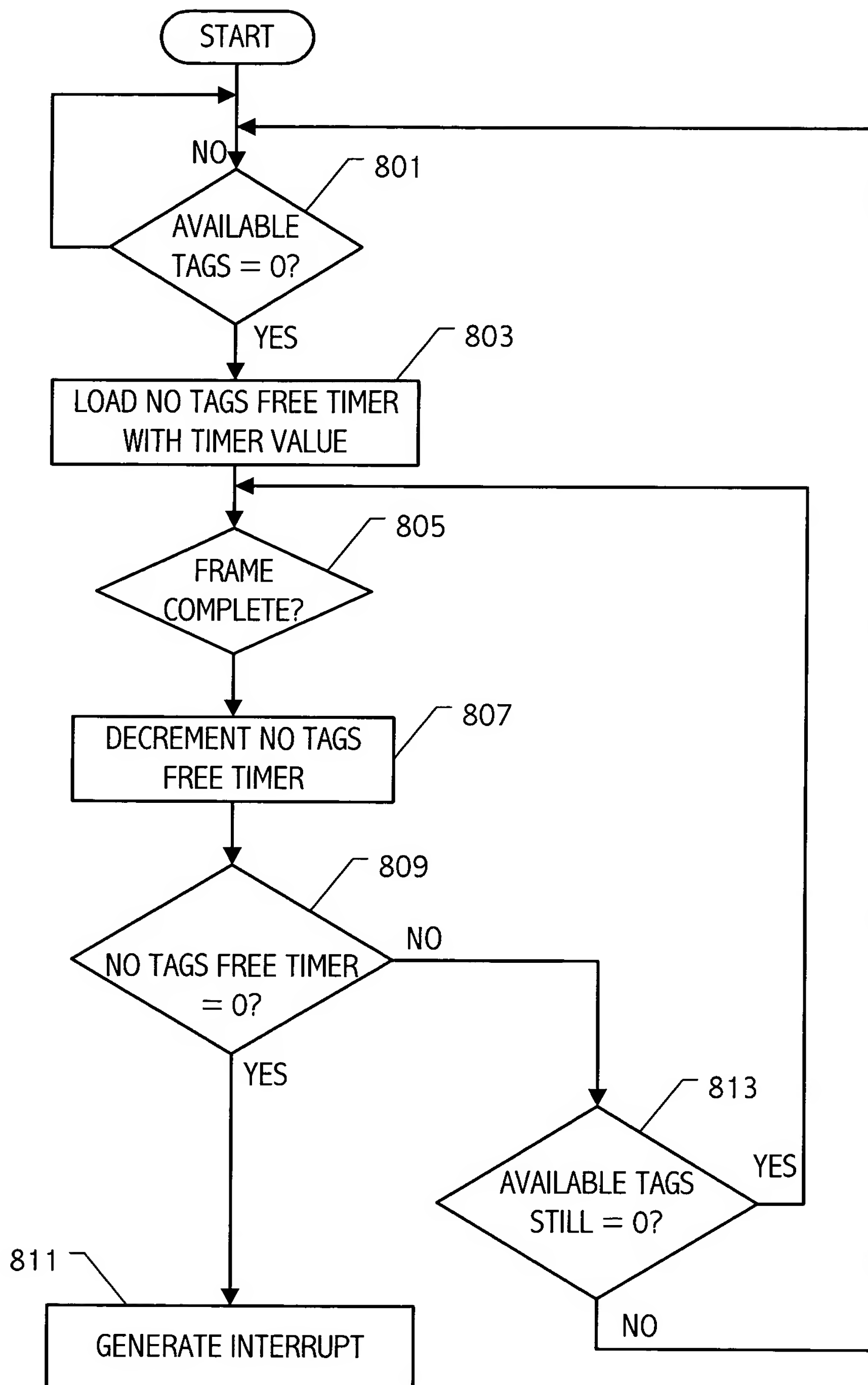


FIG. 8

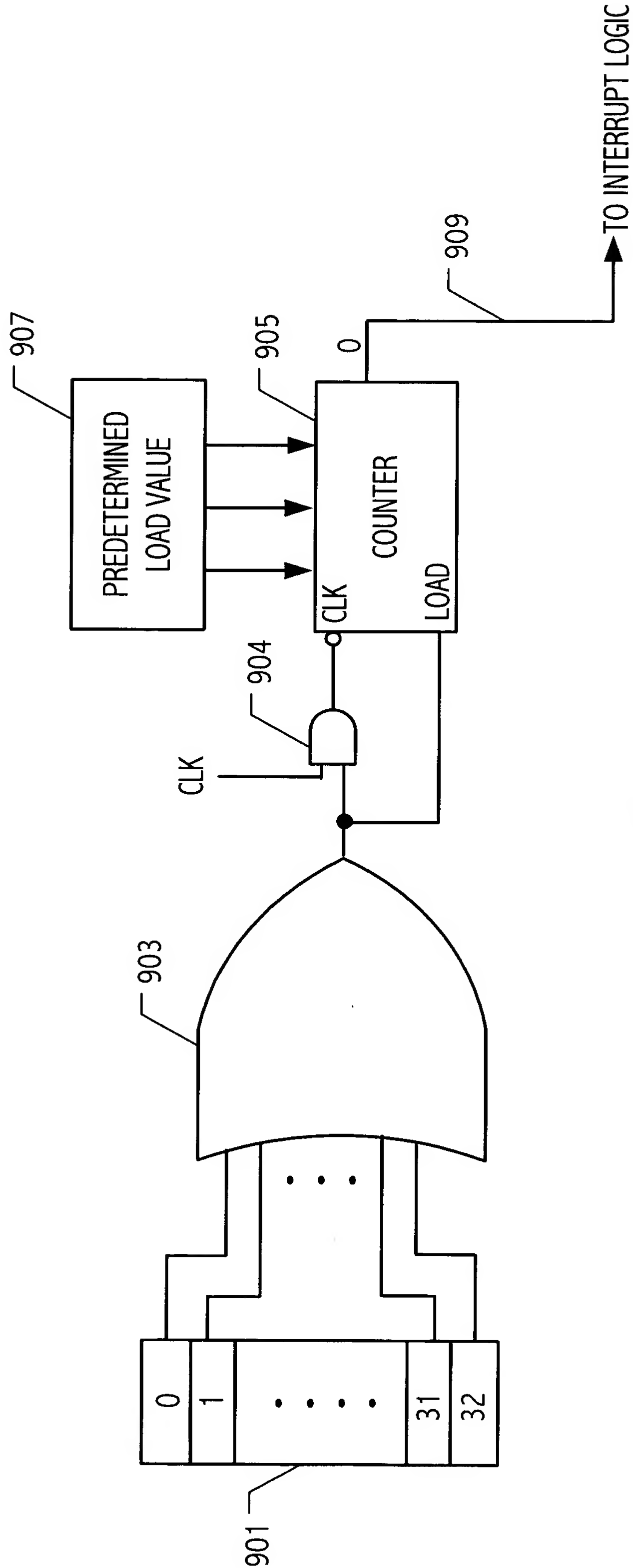


FIG. 9

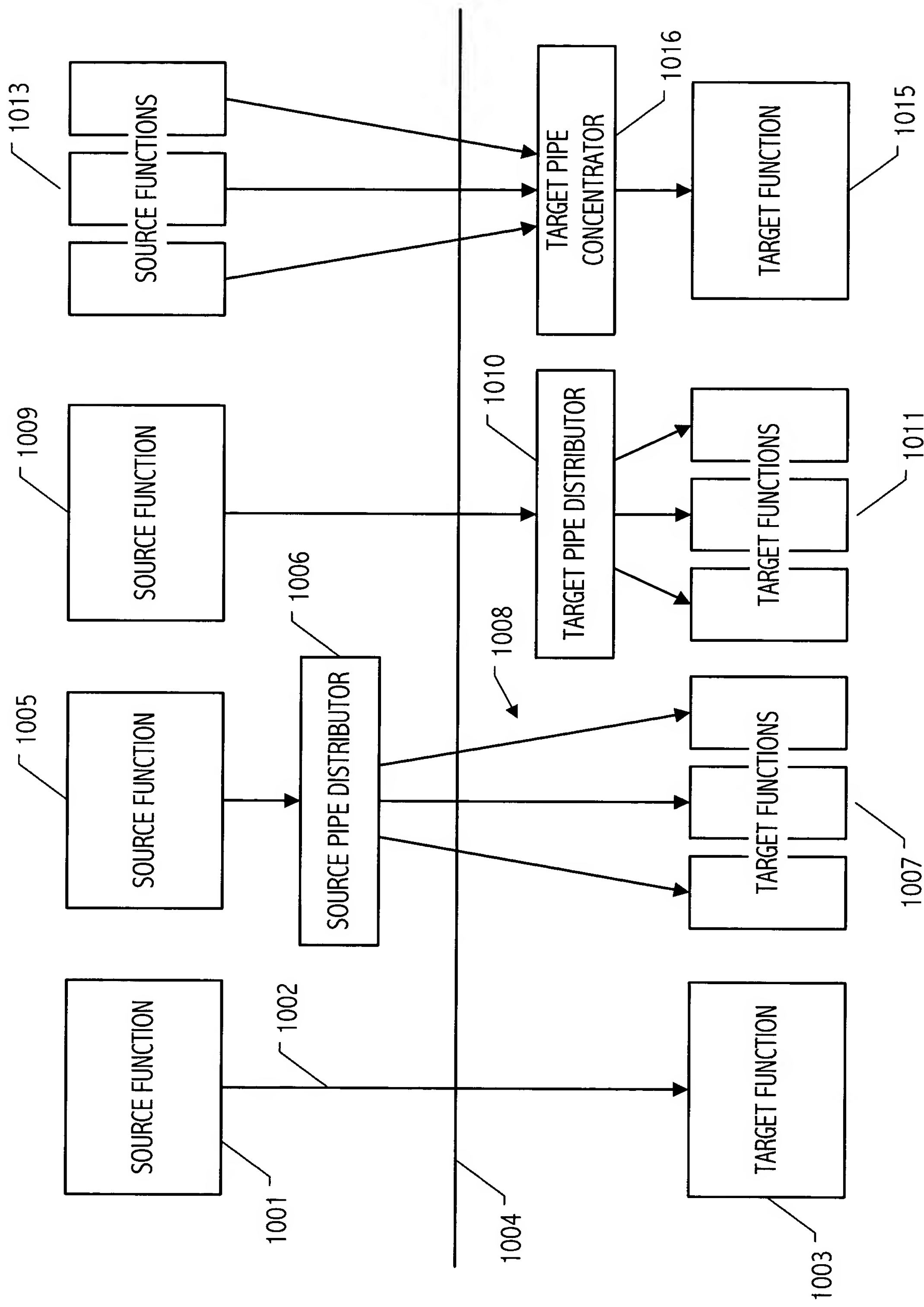


FIG. 10

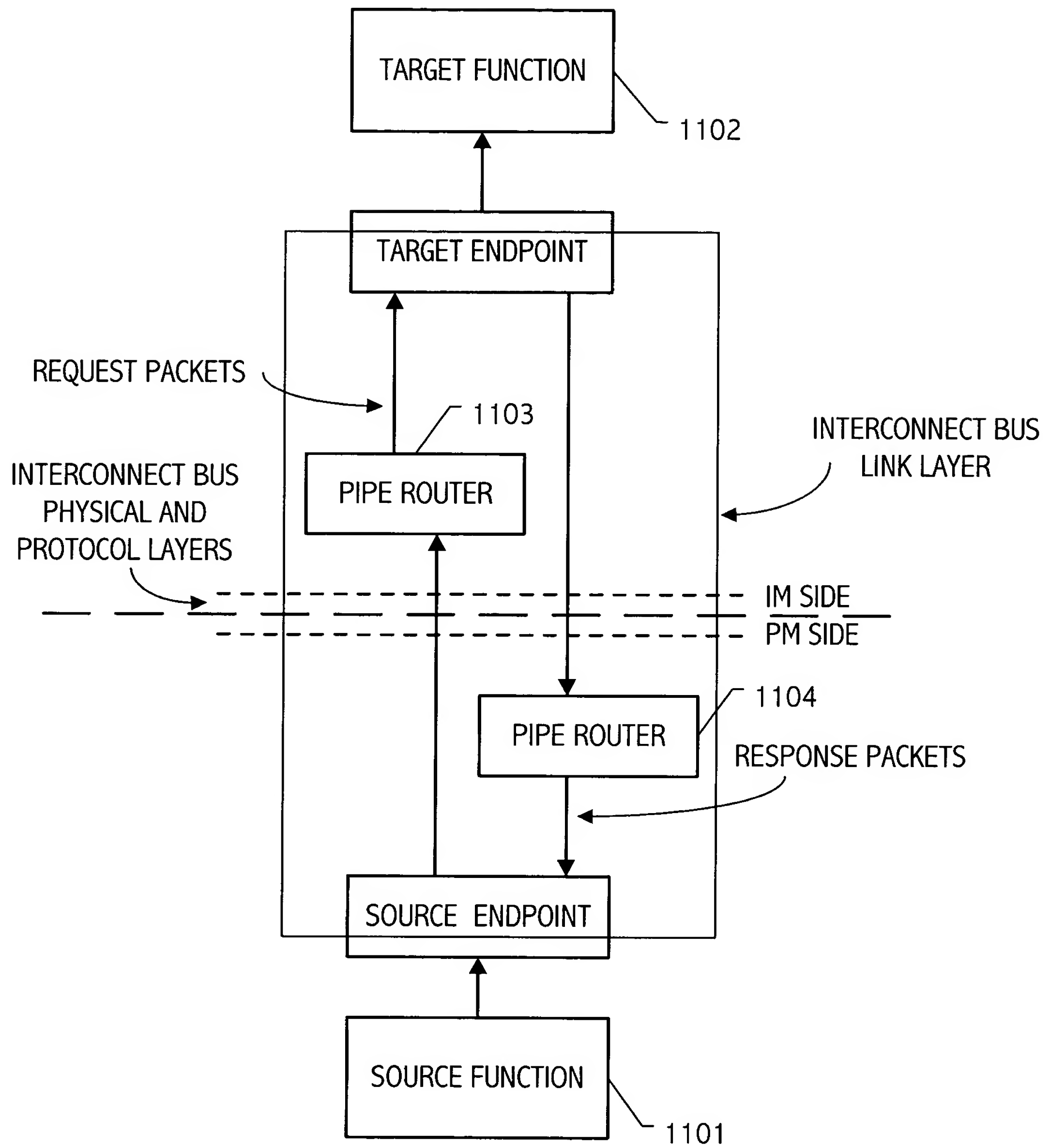


FIG. 11

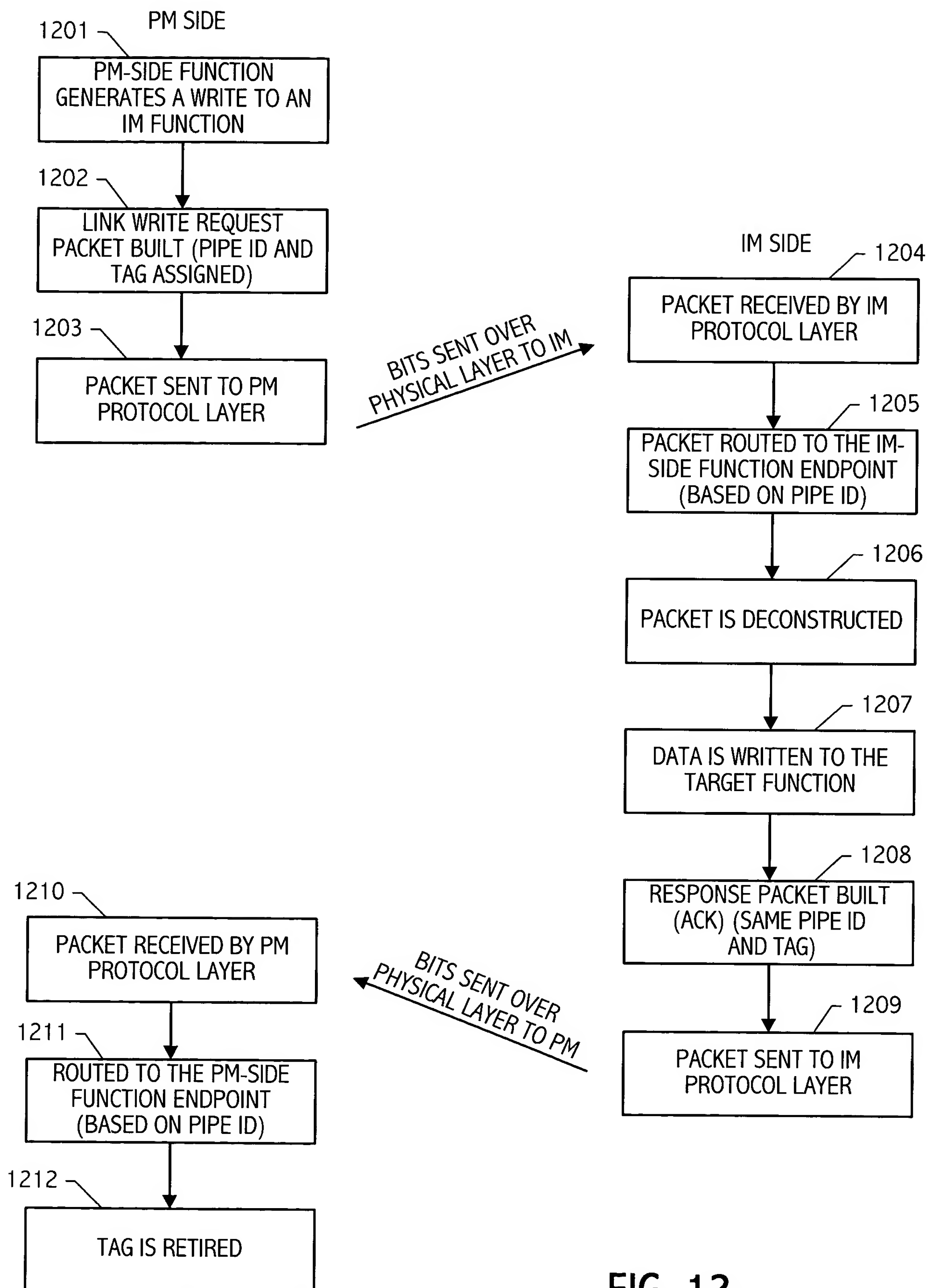


FIG. 12

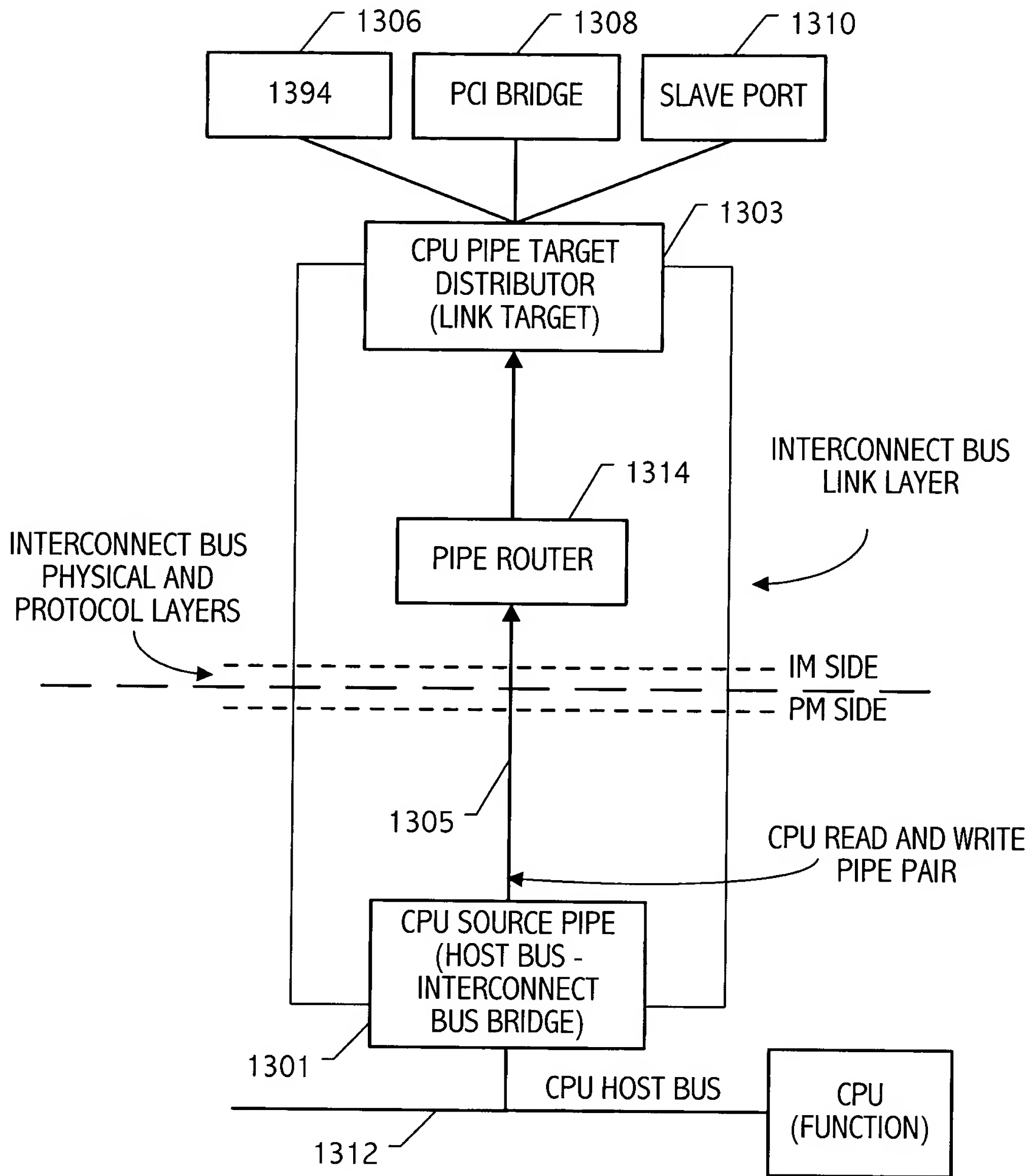


FIG. 13

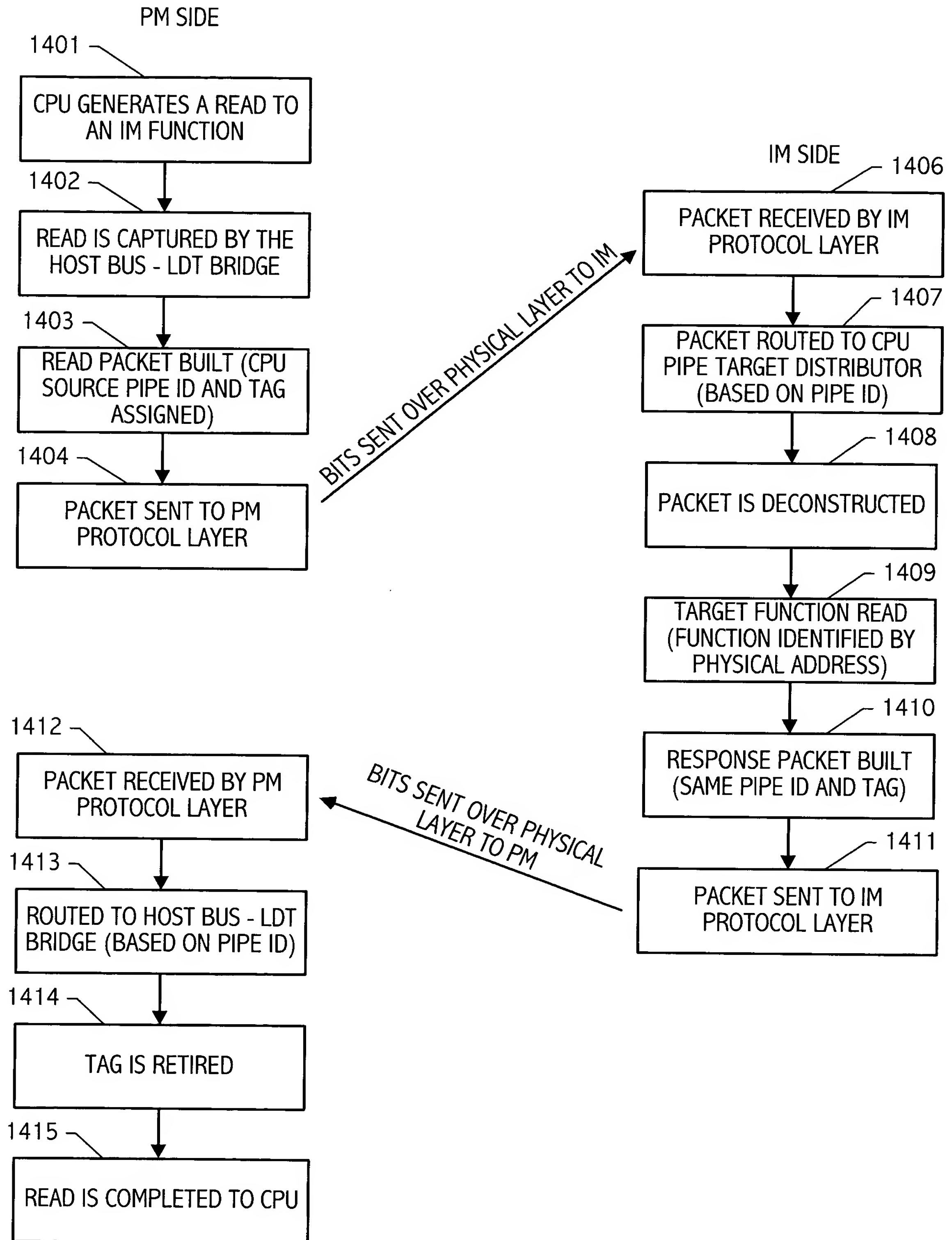


FIG. 14

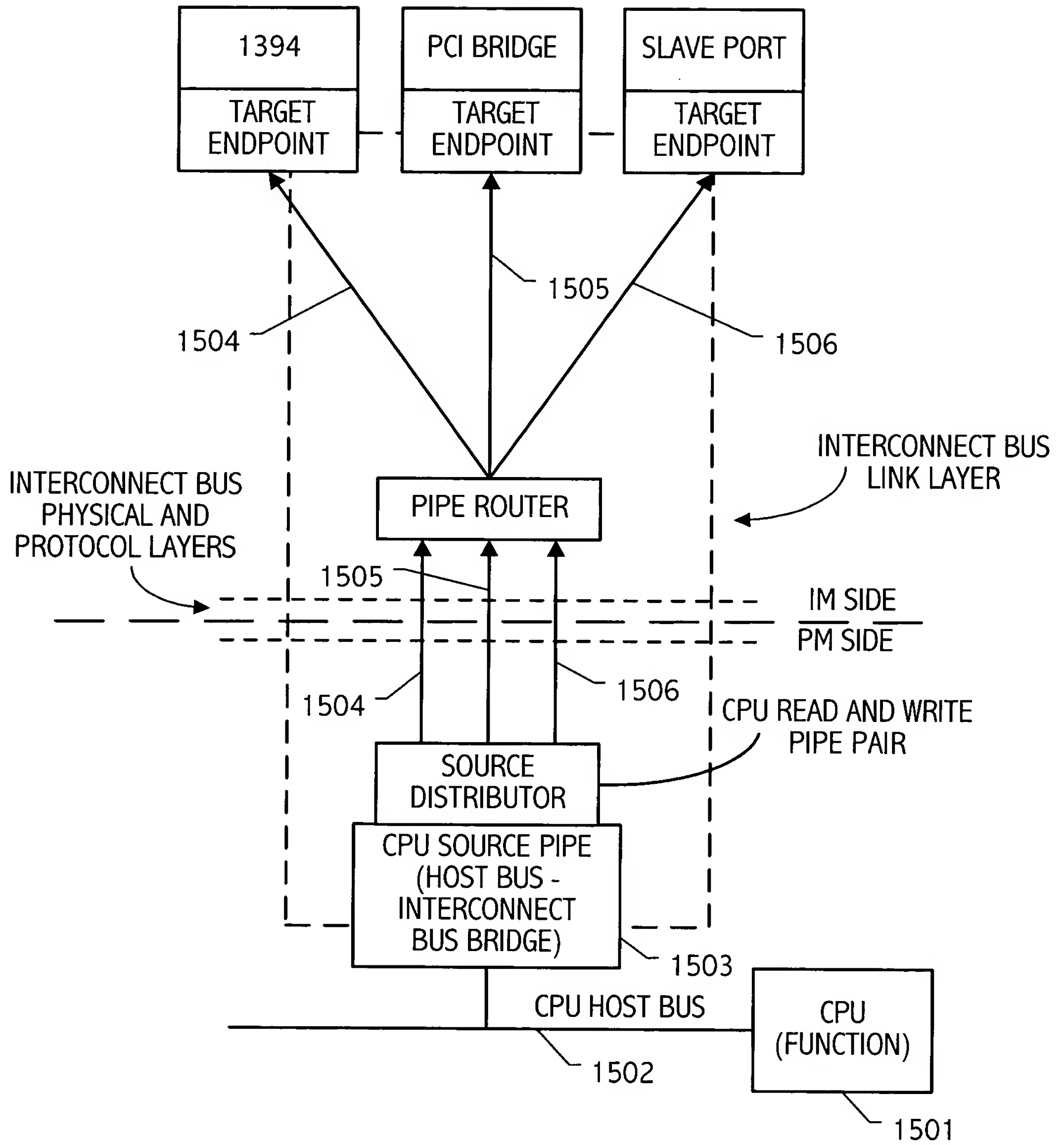


FIG.15

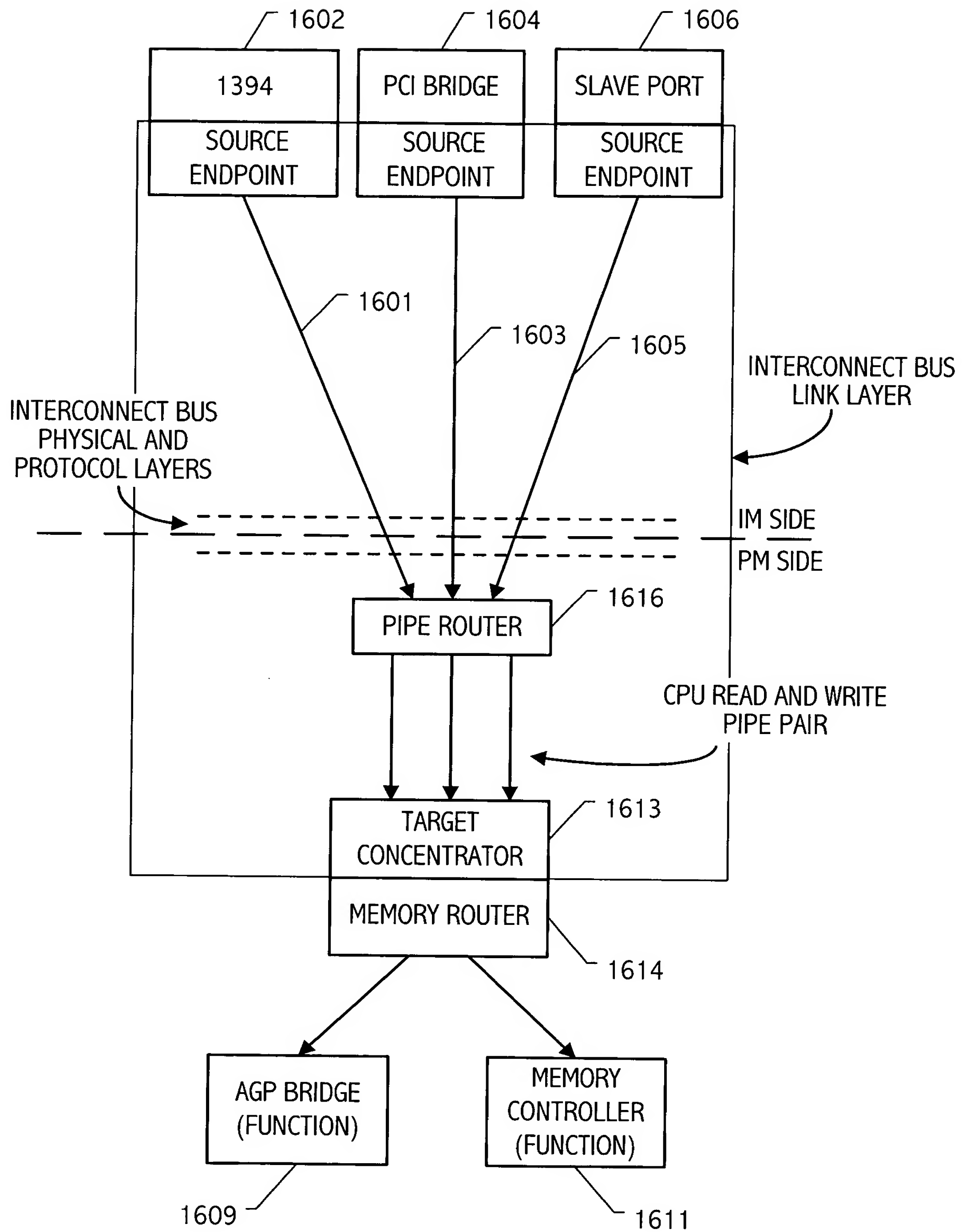


FIG. 16

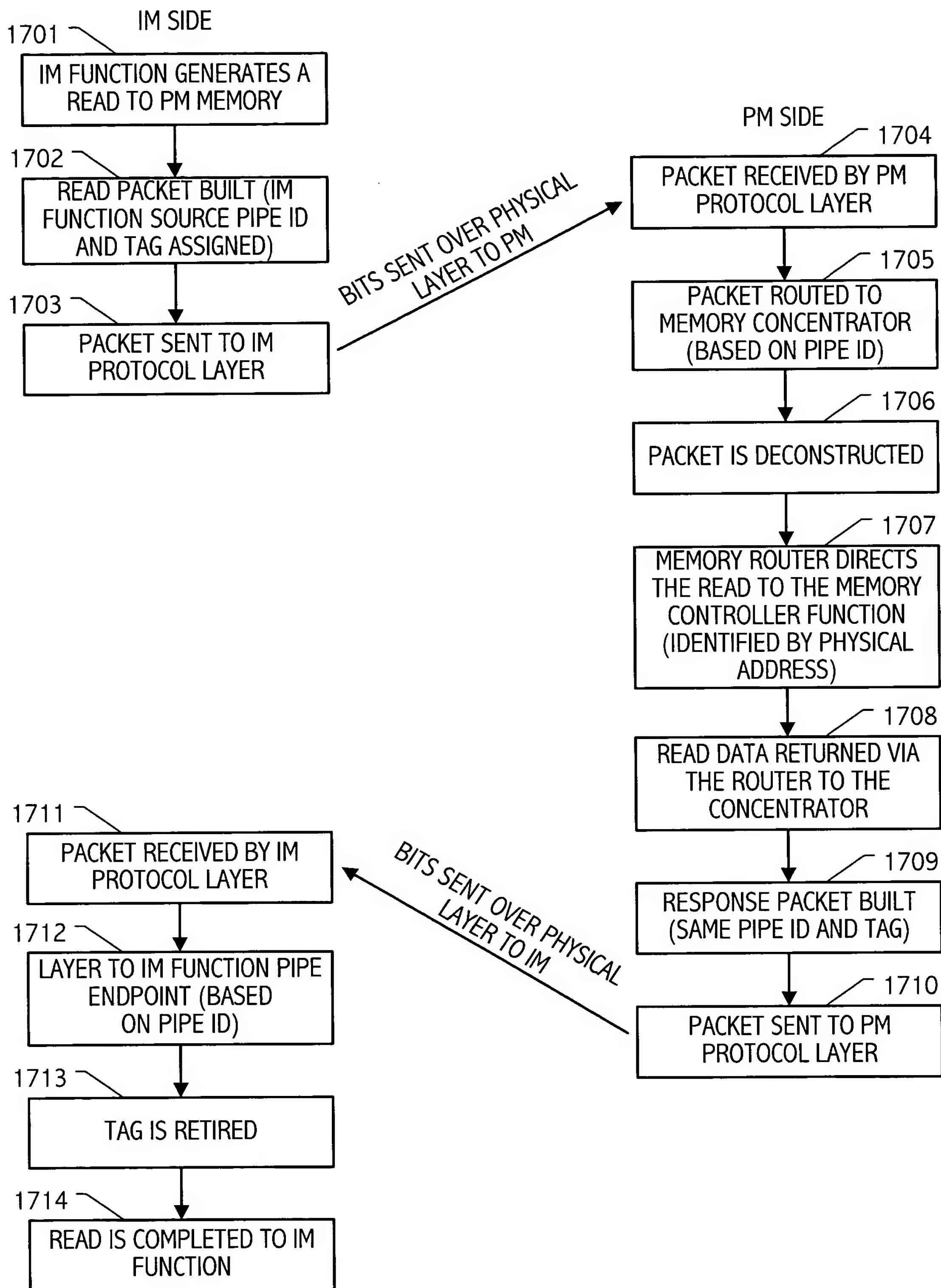


FIG. 17

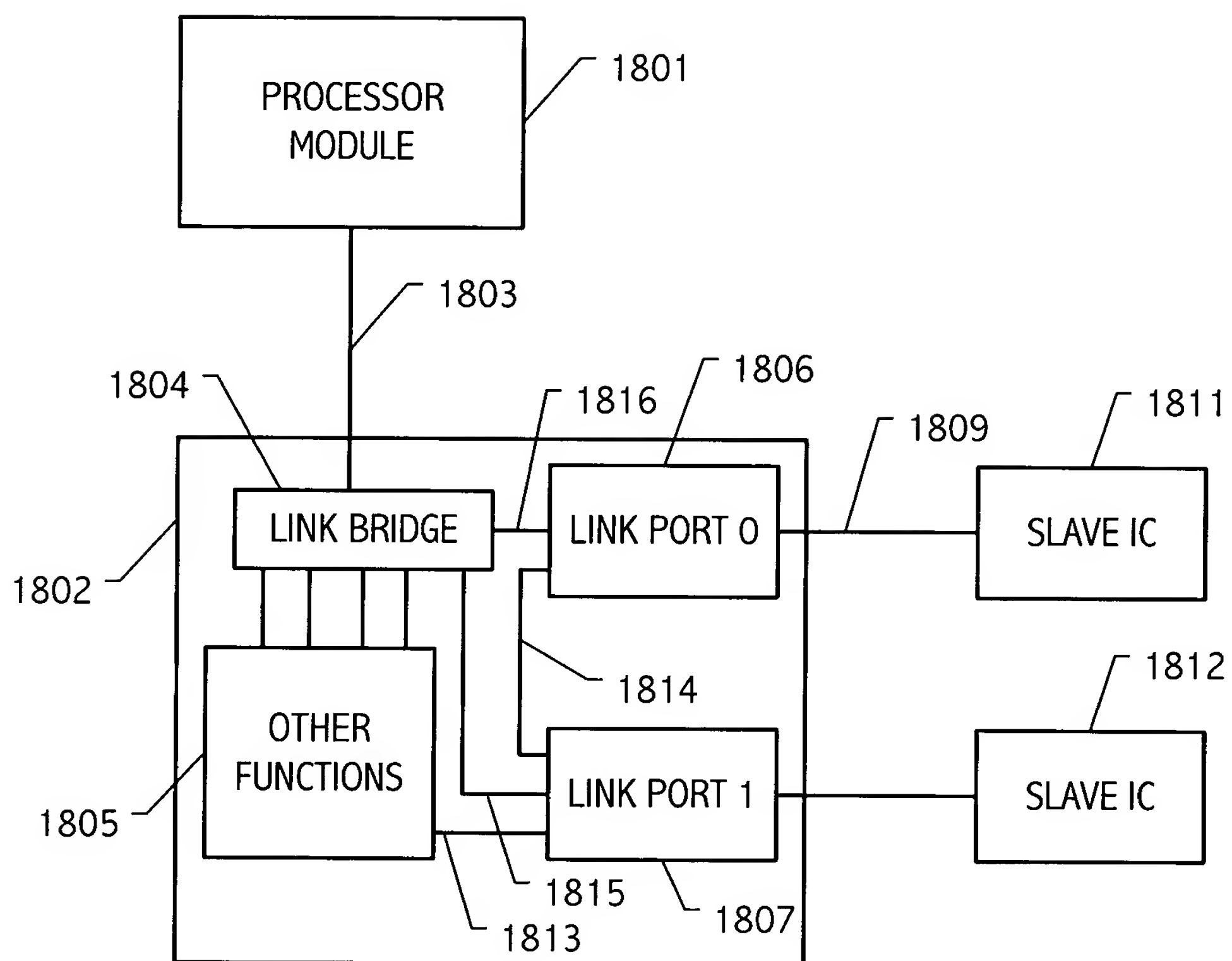
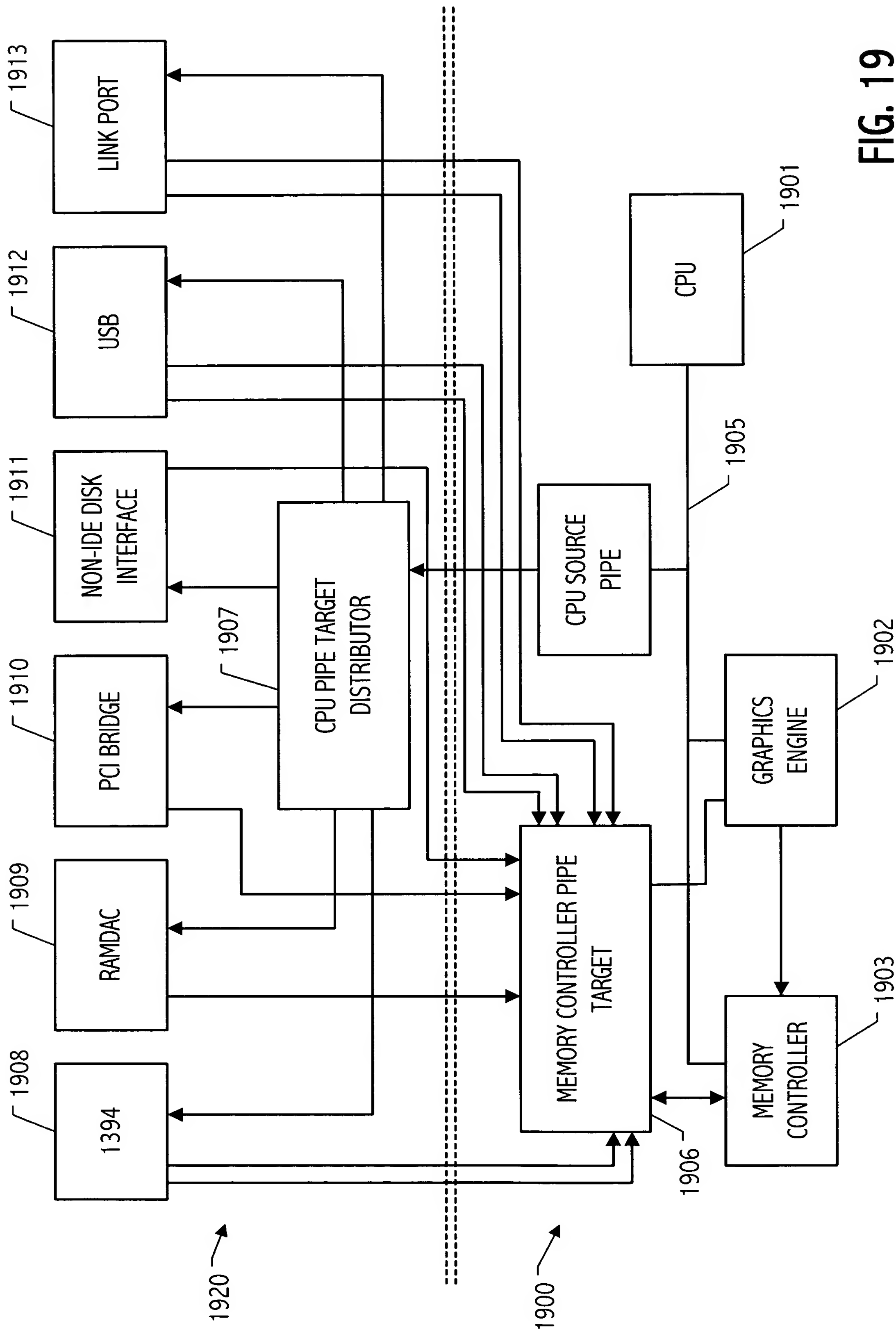


FIG. 18



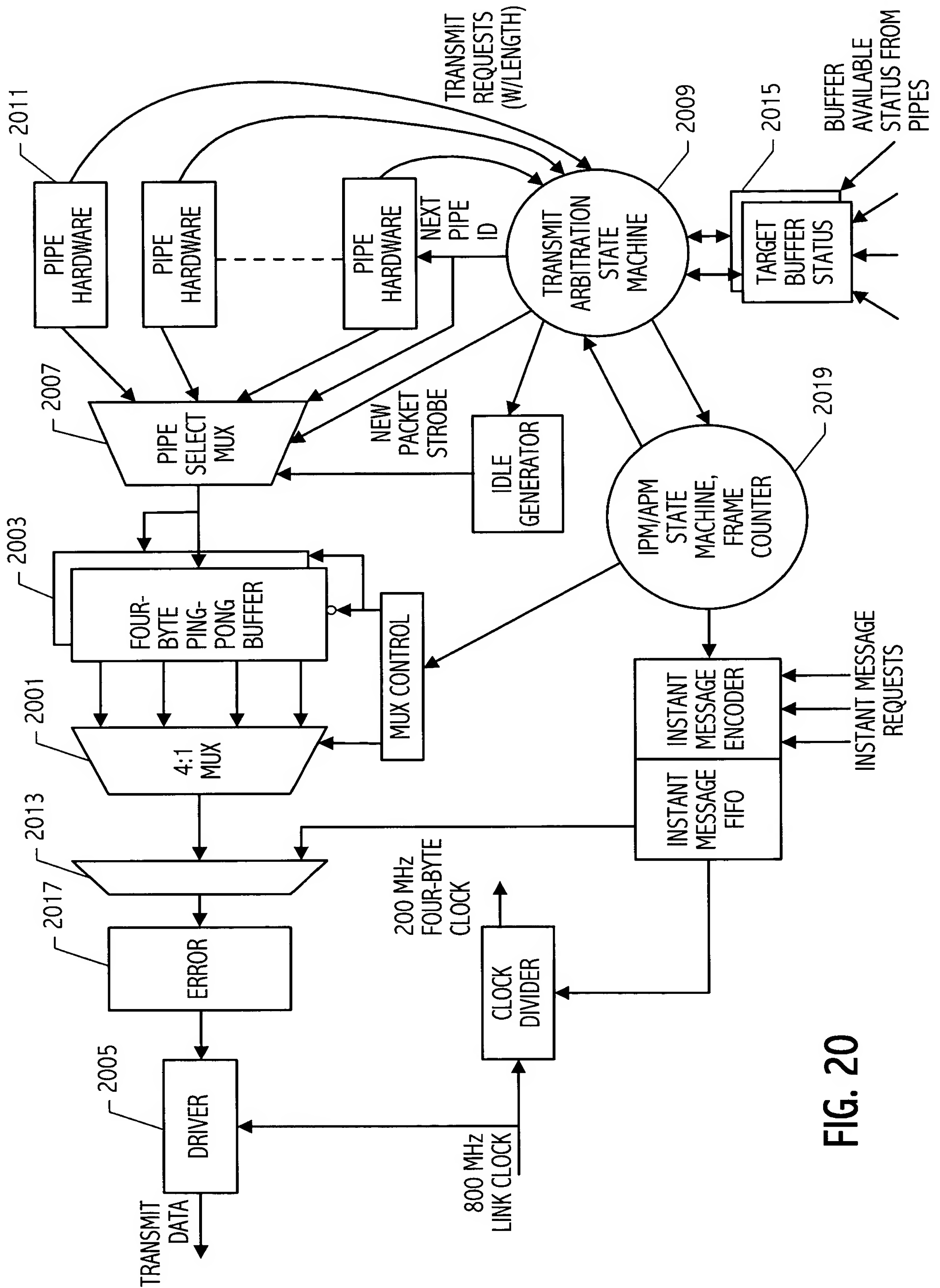


FIG. 20

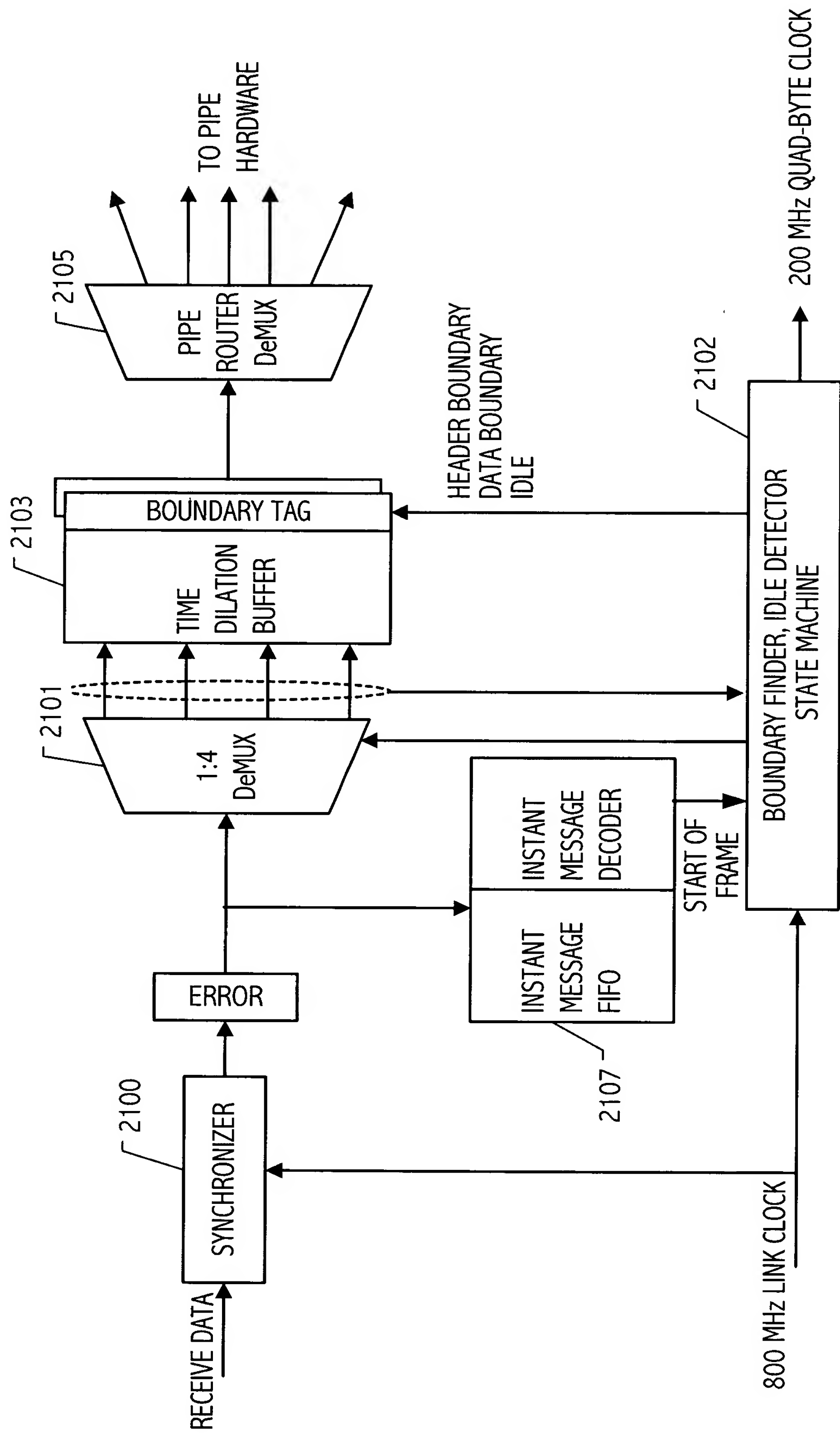


FIG. 21

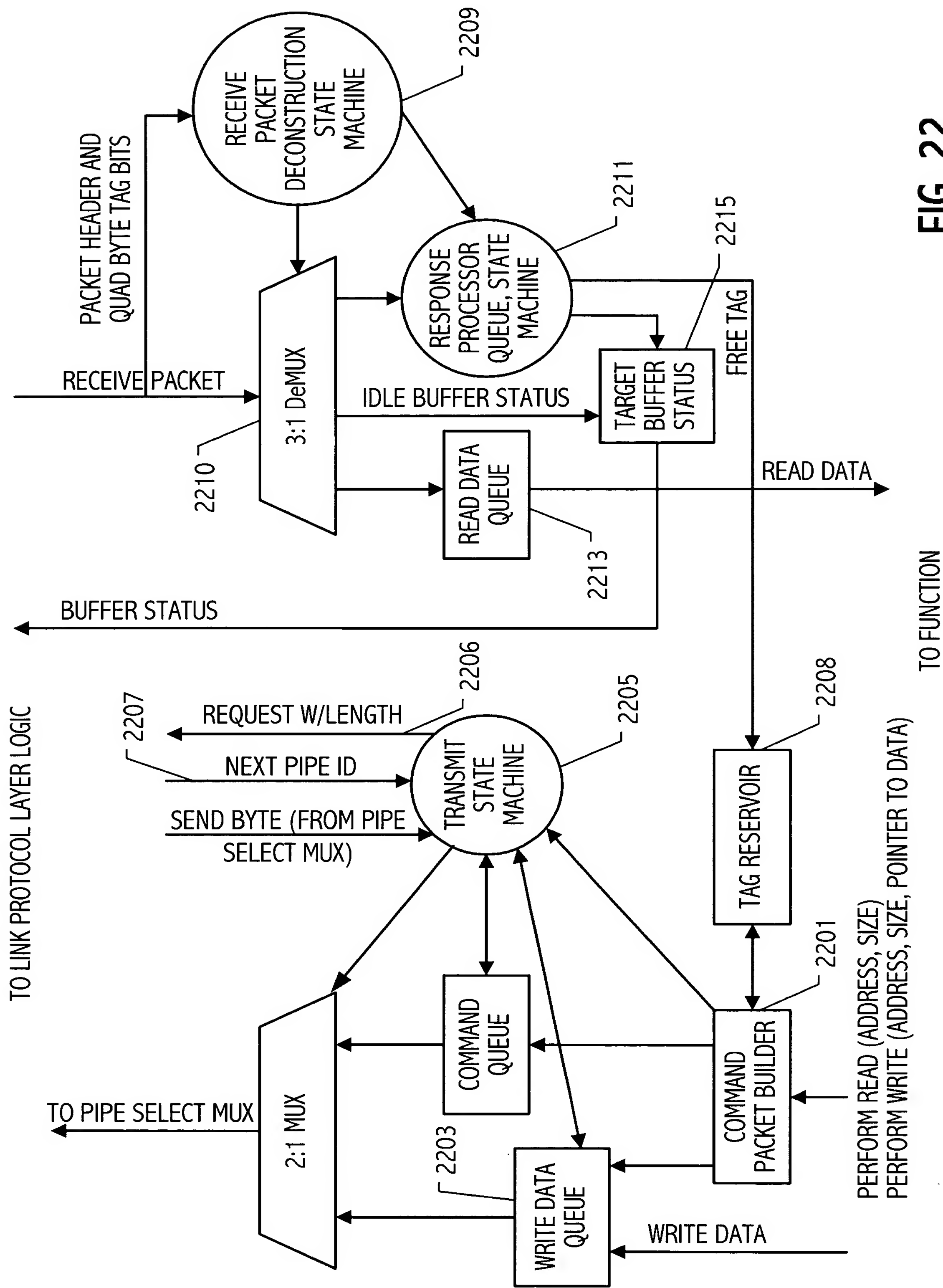


FIG. 22

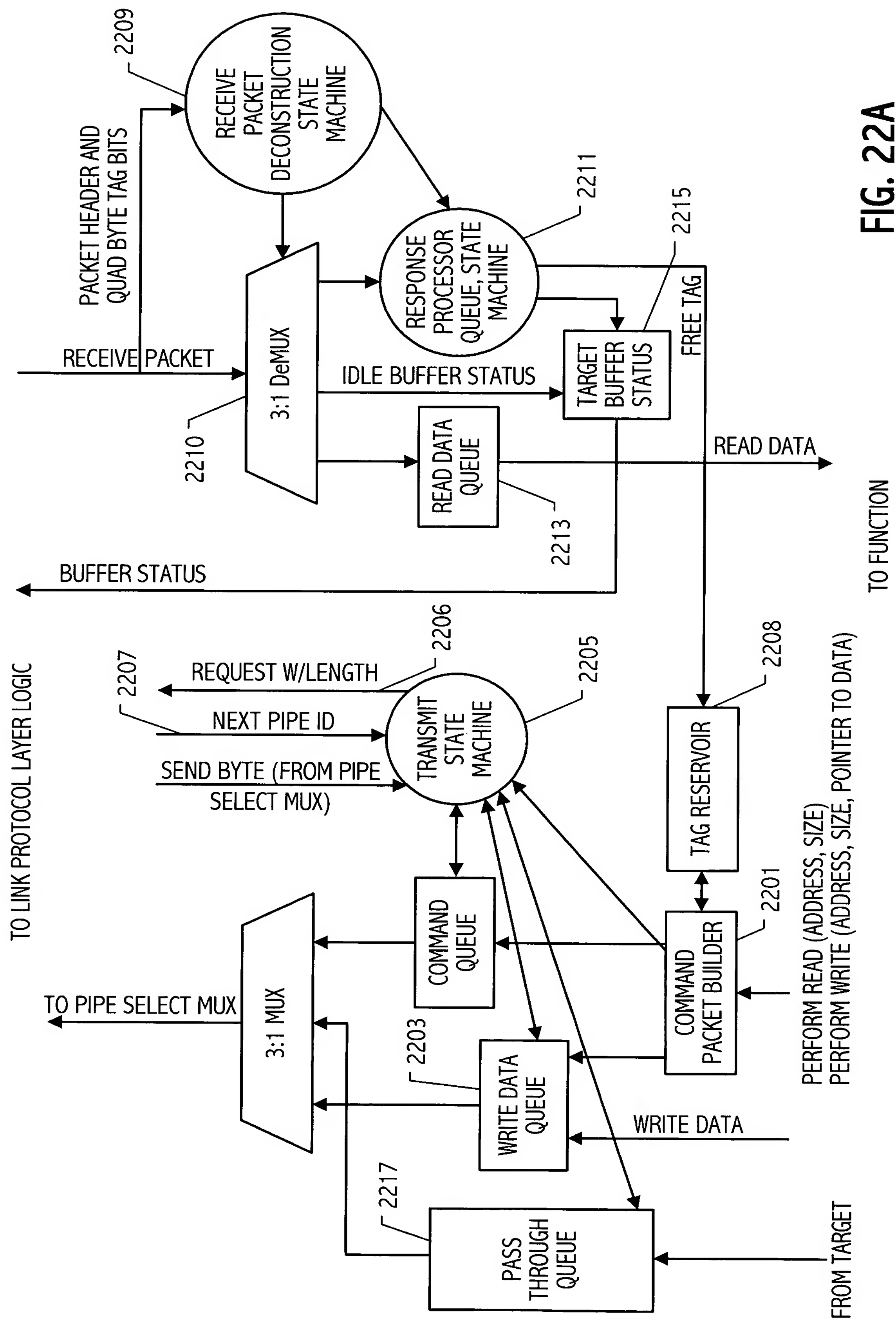


FIG. 22A

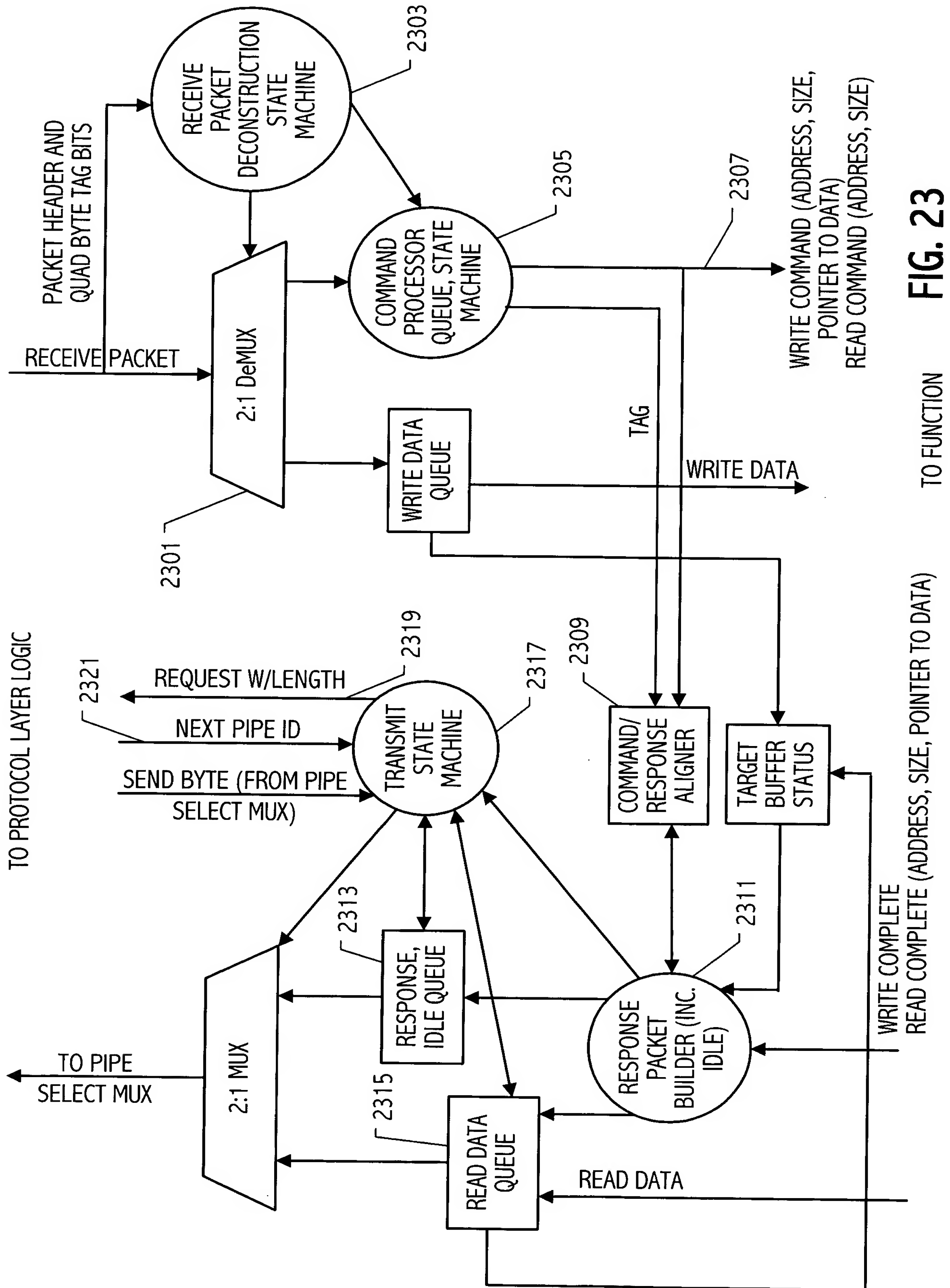


FIG. 23

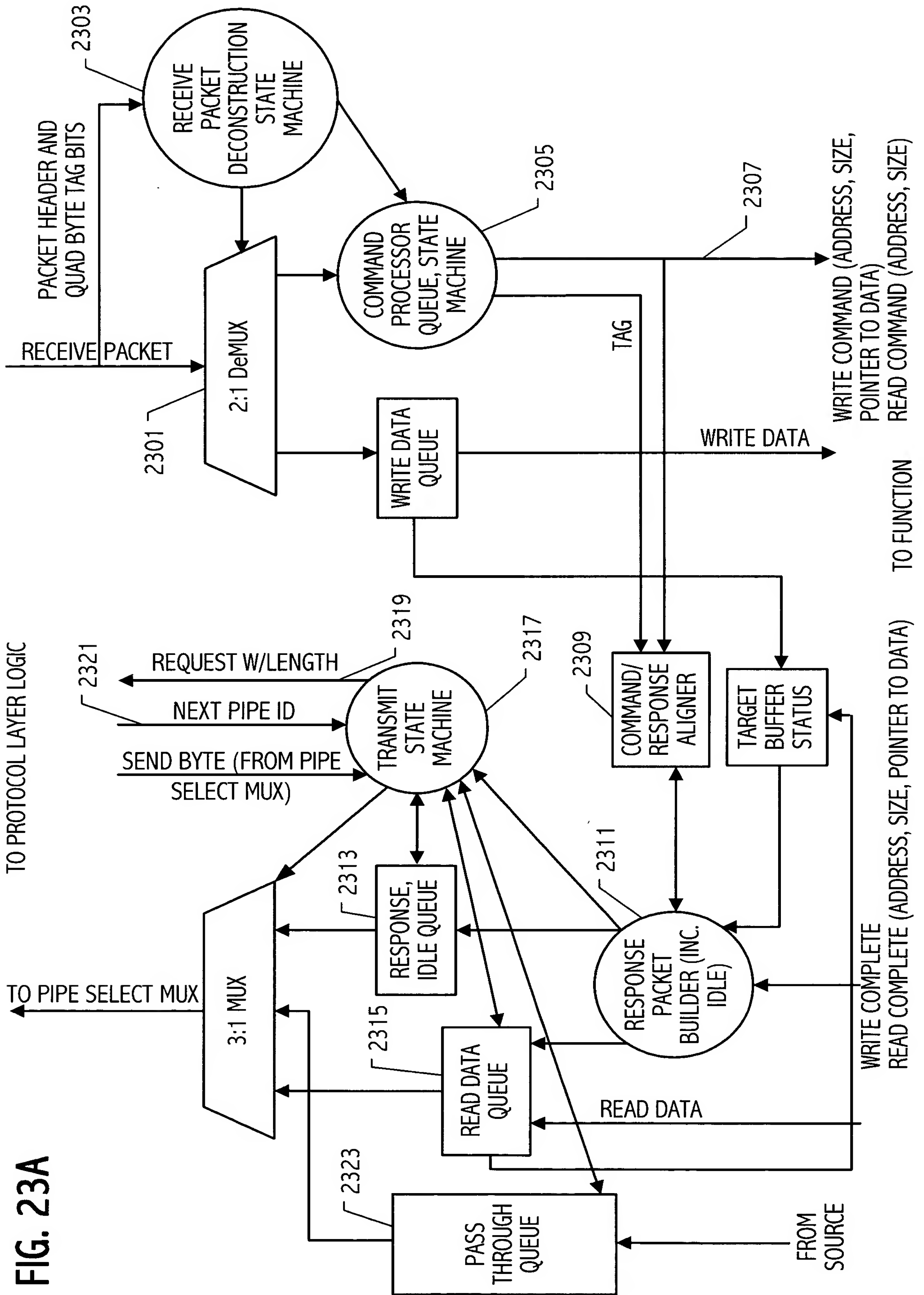
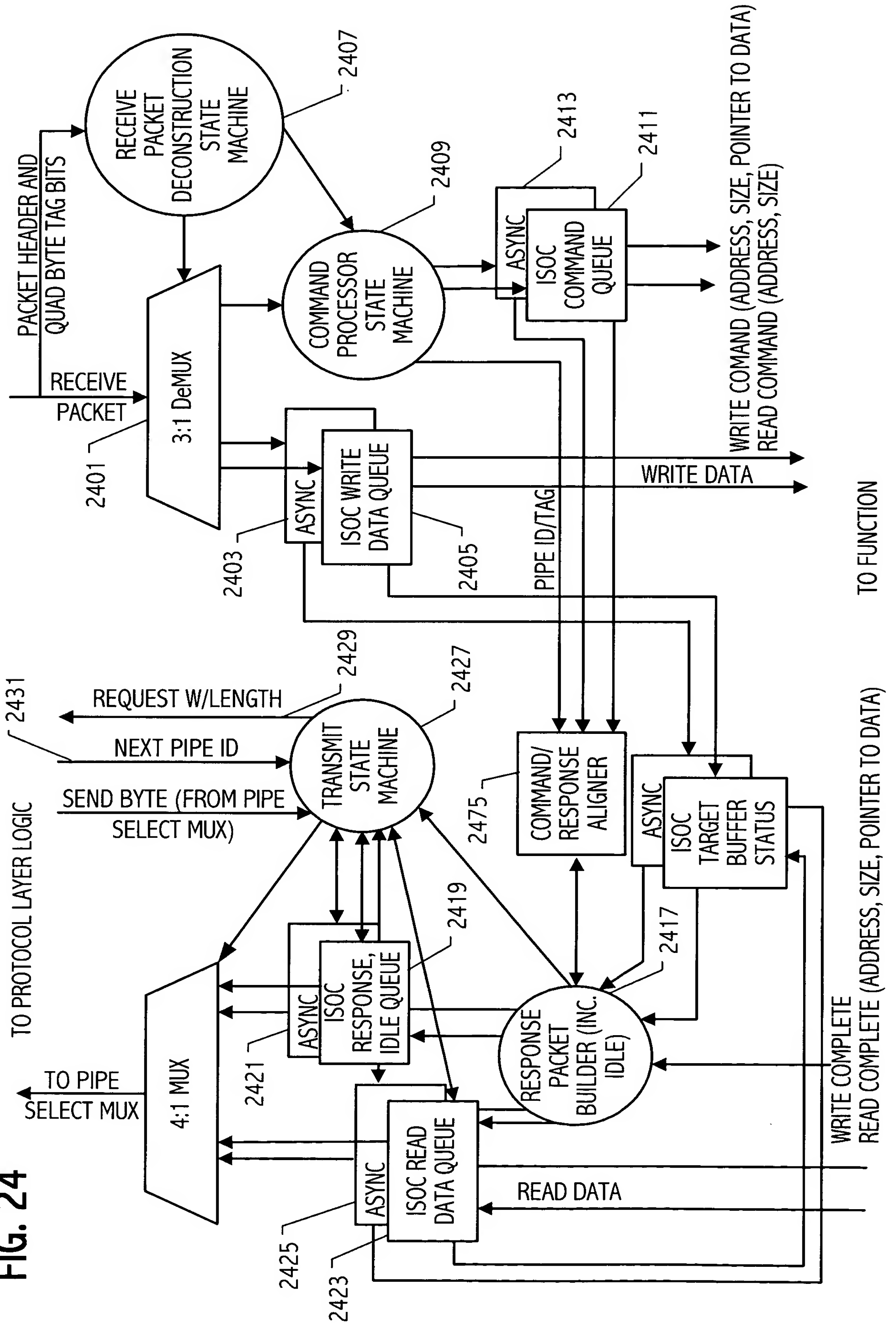


FIG. 23A

FIG. 24



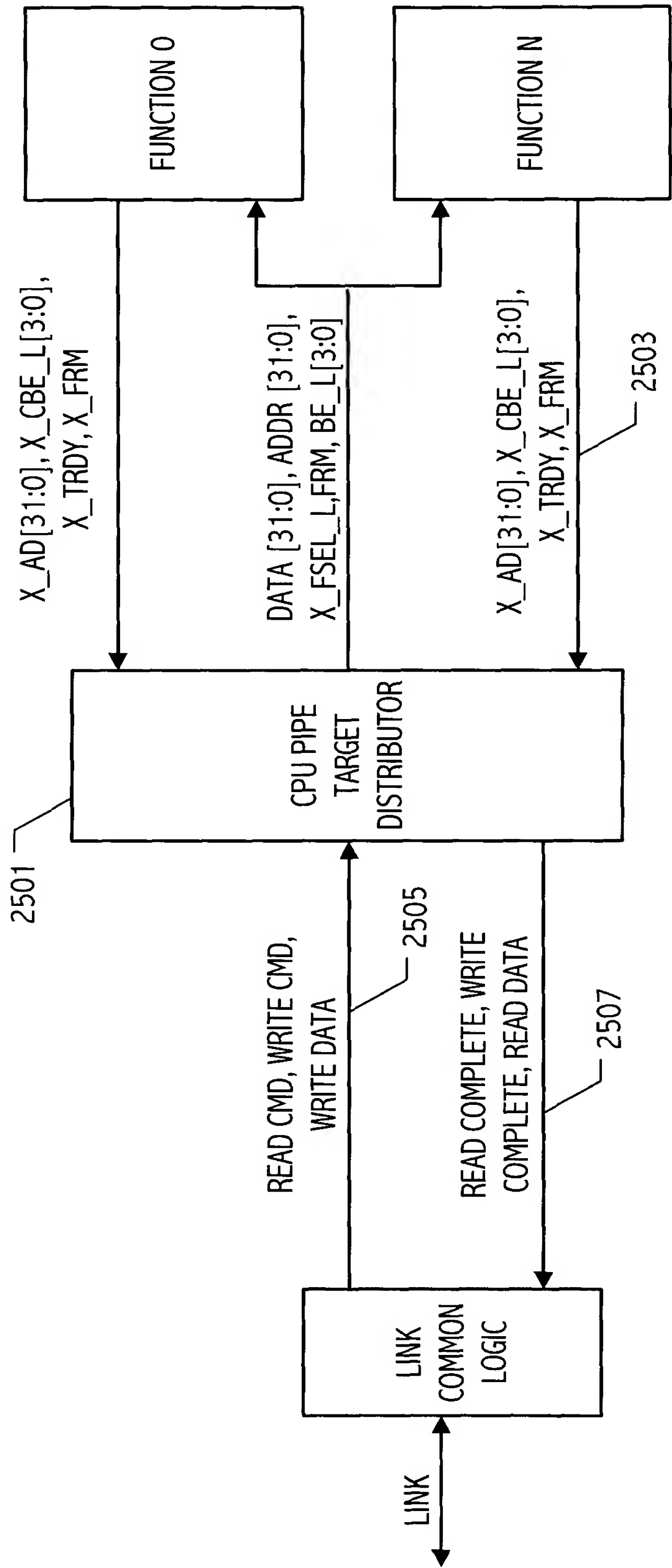


FIG. 25

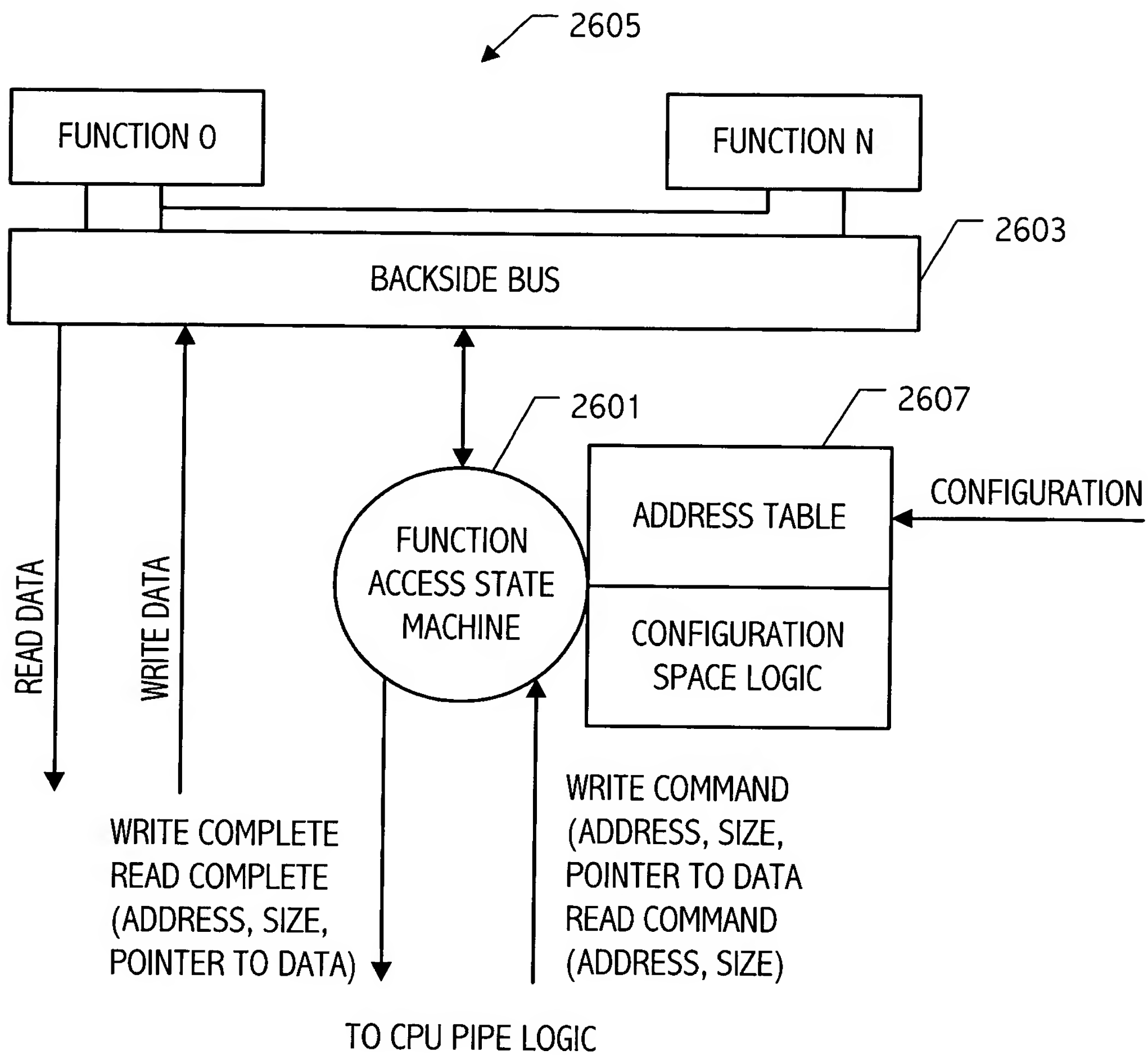


FIG. 26

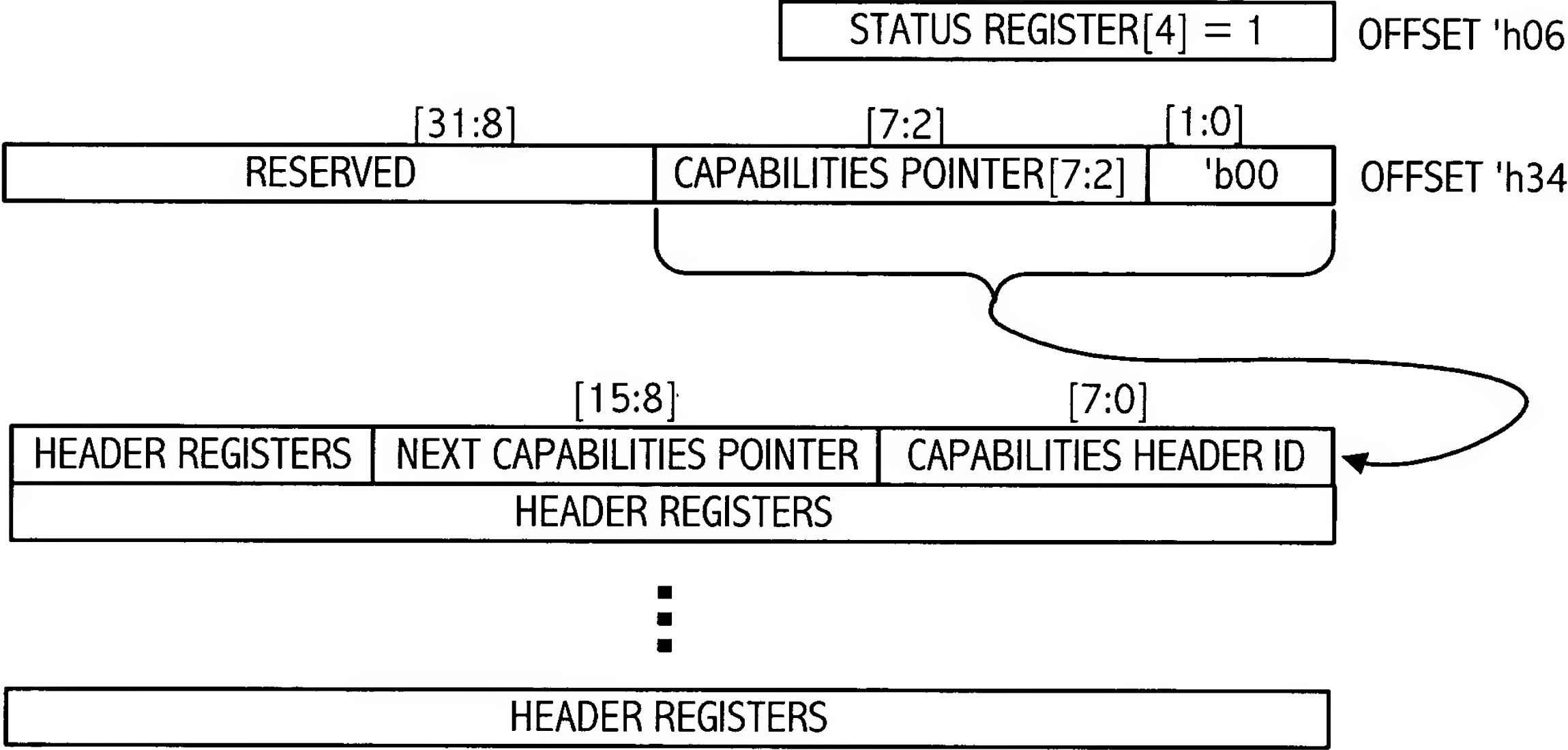
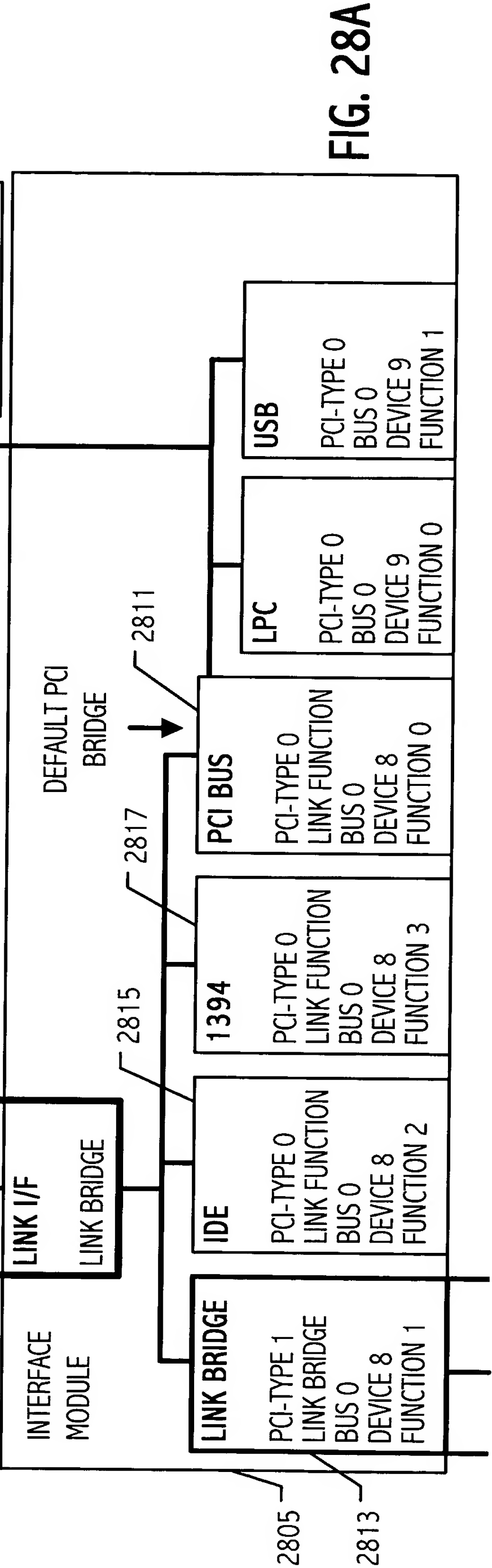
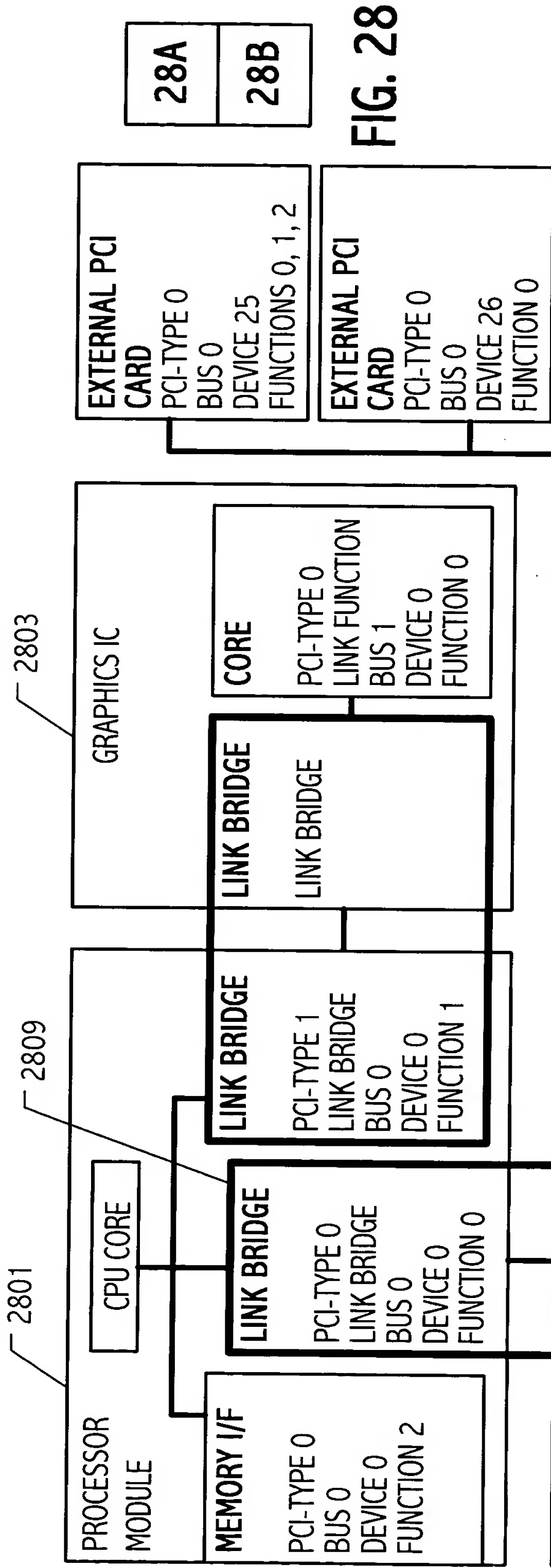


FIG. 27



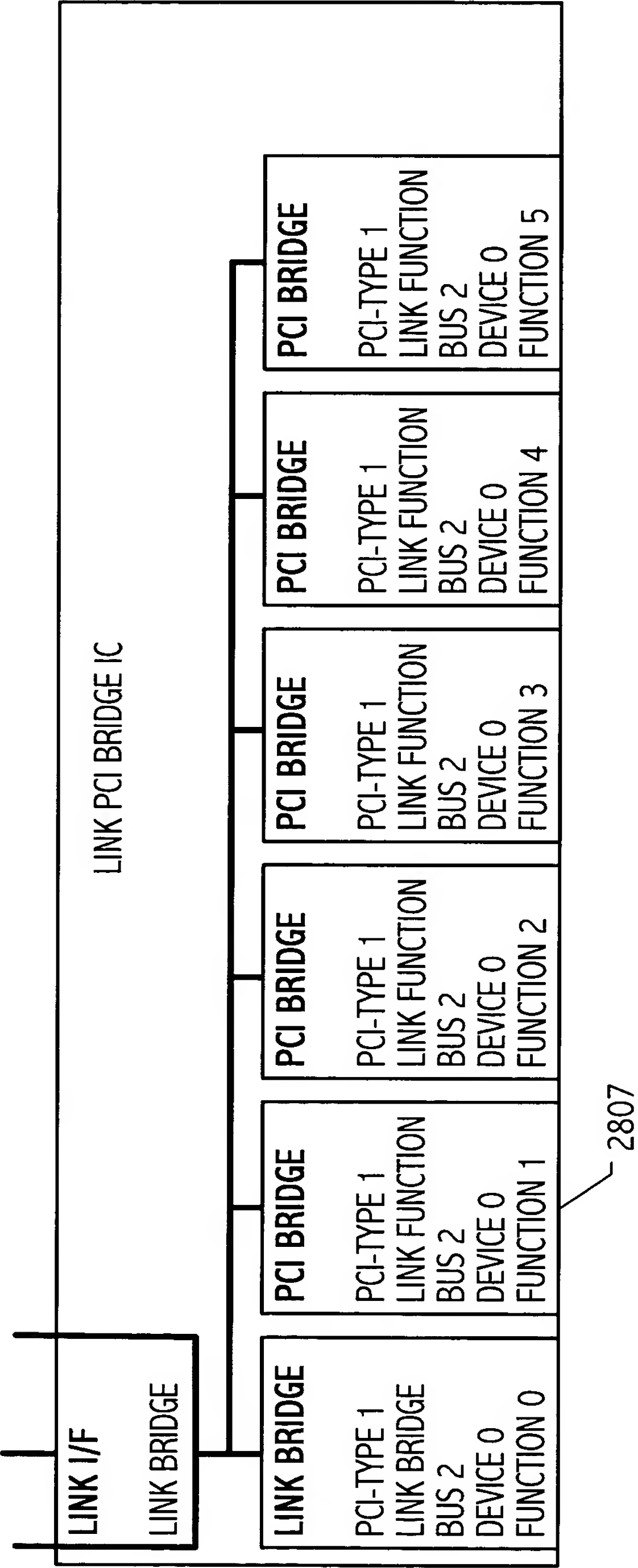


FIG. 28B

TYPE 1

DEVICE ID		VENDOR ID		00h
STATUS		COMMAND		04h
CLASS CODE			REVISION ID	08h
BIST	HEADER TYPE	LATENCY TIMER	CACHE LINE SIZE	0Ch
BASE ADDRESS REGISTERS				
SECONDARY LATENCY TIMER	SUBORDINATE BUS NUMBER	SECONDARY BUS NUMBER	PRIMARY BUS NUMBER	18h
SECONDARY STATUS		I/O LIMIT	I/O BASE	1Ch
MEMORY LIMIT		MEMORY BASE		20h
PREFETCHABLE MEMORY LIMIT		PREFETCHABLE MEMORY BASE		24h
PREFETCHABLE BASE UPPER 32 BITS				
PREFETCHABLE LIMIT UPPER 32 BITS				
I/O LIMIT UPPER 16 BITS		I/O BASE UPPER 16 BITS		30h
RESERVED			CAPABILITIES POINTER	34h
RESERVED				
EXPANSION ROM BASE ADDRESS				
BRIDGE CONTROL		INTERRUPT PIN	INTERRUPT LINE	3Ch

FIG.
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PCI TYPE 0				
DEVICE ID		VENDOR ID		00h
STATUS		COMMAND		04h
CLASS CODE			REVISION ID	08h
BIST	HEADER TYPE	LATENCY TIMER	CACHE LINE SIZE	0Ch
BASE ADDRESS REGISTERS				10h
				14h
				18h
				1Ch
				20h
				24h
CARDBUS CIS POINTER				28h
SUBSYSTEM ID		SUBSYSTEM VENDOR ID		2Ch
EXPANSION ROM BASE ADDRESS				30h
RESERVED			CAPABILITIES POINTER	34h
RESERVED				38h
Max_Lat	Min_Gnt	INTERRUPT PIN	INTERRUPT LINE	3Ch

FIG. 30

3101

UPSTREAM SIDE LINK BRIDGE REGISTERS			
RESERVED		NEXT CAPABILITIES POINTER	CAPABILITIES HEADER ID
ASYNCHRONOUS 256-BYTE COUNTER			N+'h04
ISOCRONOUS 256 BYTE COUNTER			N+'h08
IPM FRAME COUNTER			N+'h0C
ISOCRONOUS BYTE COUNTER RELOAD		MAX DETECTED ISOCRONOUS BYTE COUNT	
CLOCK FREQUENCY	MAX CLOCK FREQUENCY	ELAPSED FRAME COUNTER RELOAD	
LINK WIDTH		LINK BRIDGE CONTROL	
RESERVED			N+'h1C
DOWNSTREAM SIDE LINK BRIDGE REGISTERS			
RESERVED			N+'h20
ASYNCHRONOUS 256-BYTE COUNTER			N+'h24
ISOCRONOUS 256 -BYTE COUNTER			N+'h28
IPM FRAME COUNTER			N+'h2C
ISOCRONOUS BYTE COUNTER RELOAD		MAX DETECTED ISOCRONOUS BYTE COUNT	
CLOCK FREQUENCY	MAX CLOCK FREQUENCY	ELAPSED FRAME COUNTER RELOAD	
LINK WIDTH		LINK BRIDGE CONTROL	
RESERVED			N+'h3C

FIG. 31

3102